Single Event Upset Susceptibility Testing of the Xilinx *Virtex II* FPGA

Candice Yui[1], Gary Swift[1] and Carl Carmichael[2]
[1]Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA
[2]Xilinx Inc., San Jose, CA

I. Introduction

The Xilinx *Virtex II* FPGA is an advanced SRAM-configured, high gate-and pin-count device of current interest to many designers. The ability to reprogram and control the device while in operation make it especially favorable for use in space and avionic applications. Due to the many static memory elements and configuration memory array, FPGAs are susceptible to single event upsets that can lead to functional errors. Previously at MAPLD, results have been presented on the Xilinx *Virtex* FPGA that show sensitivity to upset of both the configuration and the user-incorporated memory elements when irradiated with heavy ions and protons [1]. Thus, a test vehicle for SEU susceptibility measurements on the next generation Xilinx *Virtex II* XQ2V1000FG256 was developed and heavy ion test runs have been conducted at the Texas A&M Cyclotron on the bulk-CMOS device for "static" configuration upsets. Heavy ion testing of the Xilinx *Virtex II* was conducted on the configuration, block RAM and user flip flop cells to determine their static single-event upset susceptibility using LETs of 1.2 to 60 MeVcm^2/mg. A software program specifically designed to count errors in the FPGA was used to reveal $L_{1/e}$ values (the LET at which the cross section is 1/e times the saturation cross-section) and single-event functional-interrupt failures. Note that a military/aerospace product built on an epitaxial layer is expected soon and similar test methods will be applied.

II. Experimental Details

A. Device Properties

The Xilinx *Virtex II* is part of the new *Virtex II* Platform series developed specifically for addressing the needs of a sophisticated System on a Chip (SoC) design in a single programmable device. The *Virtex II* offers logic performance to greater than 300 MHz, and high-density on-chip memory provides a higher overall system bandwidth. Some other features and capabilities of interest are:

- IP-Immersion Architecture: Allows complex IP based designs to incorporate large number of advanced routing resources, on-chip memories, and embedded multipliers.
- Active Interconnect Technology: Provides routing resources to accommodate for high fan-out nets typical of multi-million gate designs and enables IP portability and reuse by providing consistent and predictable high performance.
- Select I/O-Ultra & 840 Mbps LVDS: Allows each user I/O pin to be individually programmable for 19 single-ended I/O standards or six differential I/O standards.
- XCITE Technology (digitally controlled impedance): Eliminates the reflections and ringing of mismatched I/Os through dynamic adjustment of impedance and allow maximum I/O bandwidth while reducing board space and cost.

In addition, the 12 on-board Digital Clock Managers (DCMs), embedded 18x18 multipliers, and SRAM-based in-system configuration make this device attractive for use in many telecommunication, wireless, networking, video and DSP applications, including those in space.

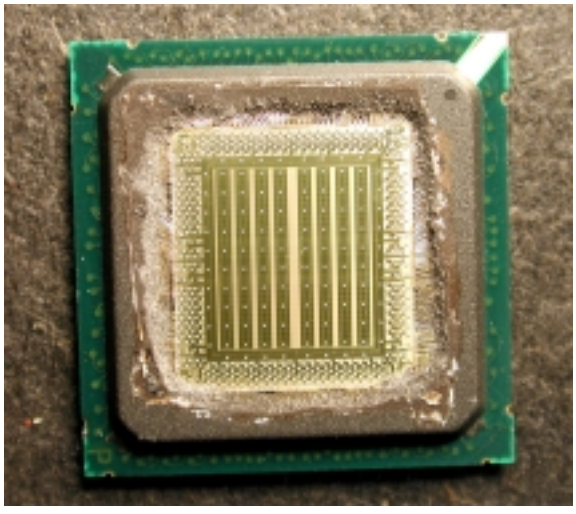

Figure 1: *Virtex II* XC2V1000 is etched to expose the die more directly to heavy ions for ground testing. The individual blocks seen here are the internal configurable logic blocks (CLBS) situated among rows of block SelectRam, multipliers, input/output blocks (IOBs) and other *Virtex II* architectural components. Die size is approximately 380 x 380 mils.

The research done in this paper was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration (NASA), under the NASA Electronic Parts and Packaging Program (NEPP), Code AE and with the collaboration of Xilinx Inc.

Candice Yui and Gary Swift are Radiation Effects Engineers at the Jet Propulsion Laboratory located at 4800 Oak Grove Dr. Pasadena, CA 91109. Carl Carmichael is the Technical Sales Engineer at Xilinx Inc. located at 2100 Logic Dr. San Jose, CA 95124.

The device chosen for this study is the *Virtex II* XC2V1000. Device was procured as a commercial 256-pin wire-bond standard ball gate array (BGA) package. The *Virtex II* XC2V1000 consists of 1M system gates with a core voltage of 1.5V. It is fabricated on a 0.15µm / 0.12µm CMOS 8-layer metal process and it's architecture-optimized for high speed with low power consumption. This *Virtex II* includes 40 block RAMs, 432 maximum I/Os, and 4.1M configuration bits [2]. Devices were chemically etched on the top to expose the die and help improve ion range (Fig. 1). A cross section of the device was also done to determine the depth of each of the underlying layers (Fig. 2, Table 1).

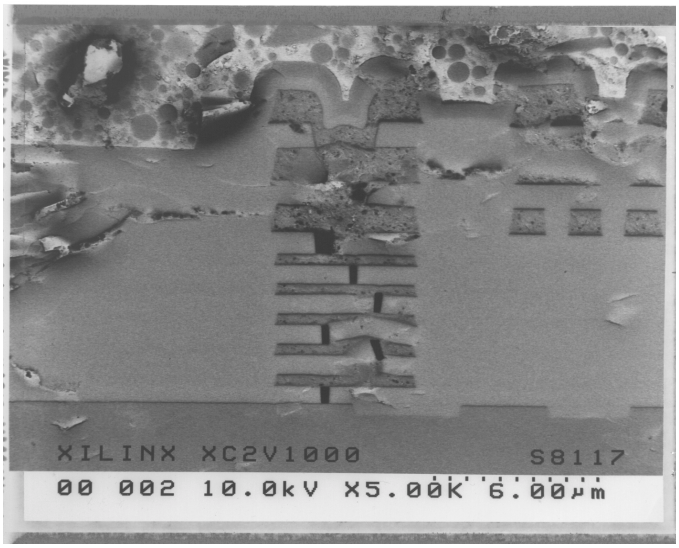

Figure 2: The over-layers materials and their thickness was taken into account for beam runs with the aid of a cross section produced by JPL's Failure Analysis Lab.

Table 1. Intervening Material Descriptions Used in First Ion Test for Adjusting Beam LET

Layers		
50,000u	Air	Foil to DUT
25.4u	Aramica	Exit Foil
7.2u	SiO2	Lumped Device Over-layers
5.7u	Al	
1u	Polyimide	
0.3u	Ti	
310u	Epoxy	Residual Package

B. Irradiation Facility

Heavy-ion irradiations were performed at the Cyclotron Institute's Radiation Effects Facility at Texas A & M University in College Station, Texas. Their facility consists of a set of high energy (25 MeV/nucleon) noble gas beams (Ne, Ar, Kr, and Xe) that provide a broad range of linear energy transfer (LET) (2-63 MeV/(mg/cm^2)) and good penetration depth (254 to 790 microns). The ions Neon, Argon, Krypton, and Xenon were used for this experiment to obtain LETs from 1.21 – 61.3 MeV/(mg/cm^2). All tests were performed in air. The non-active over-layers were defined and the beam control software calculated the LET incident on the active Silicon.

C. Test Procedure

Current SEU characterization of the Virtex II FPGA is composed of data collected from three different static tests. Here "static" means the test design was not clocked during irradiation. Note that the total cross section in a space application is expected to have some dynamic susceptibility that would add to the static susceptibilities reported here. The three different static tests are static configuration memory test, static configuration memory and block RAM test and static configuration memory, block RAM and flip-flops test. The results of the last two are reported together. All three tests gave relatively consistent results; the latter tests refined visibility and coverage. The purpose of each of these tests was to determine the number of upsets in the configuration, block SelectRam and flip flops/latches cells in a more efficient manner with each successive test. The test platform for each test consisted of a *HW-AFXBG256-200* prototype board connected to a host PC running custom test software via Xilinx' MultiLinx cable or the Xilinx parallel III, JTAG cable (Fig. 3).

1) Static Configuration Memory Test

This test comprised of extracting only configuration upsets using Xilinx IMPACT device programming application to configure and verify the device through the parallel III JTAG IEEE cable. Immediately following after each beam run, 'verify' was performed to determine the number of differences in the configuration memory.

2) Static Configuration, Block SelectRam Test& Flip-Flops

The second test captures static configuration and block SelectRam data through a MulitiLinx cable connected directly to the DUT through modifications made to the prototype board. A specifically designed C++ based application named FIVIT (Fault Injection and Verification Tool) test software was used to configure the DUT and readback SEUs in the memory cells. A screen capture of the program is included (Fig. 4). In addition, an HP6629A digital power supply was used to provide 3.3 V to the board and 1.5V to the FPGA. A separate laptop was connected to the HP6629A to strip chart the two voltage and current readings. The third and most current setup is identical to the static configuration and block SelectRam test described previously with the exception that more capabilities were added to FIVIT. New features of FIVIT include the ability to set all flip-flops to either '1s' or '0s', capture their data, as well as read and write to configuration registers such as the command register (CMD), frame length register (FLR), configuration option register (COR), masking register for CTL (MASK), control register

(CTL), frame address reader (FAR), CRC register, and the status register (STAT). Another useful utility added to FIVIT is the option of reading and writing to configuration registers through either the MultiLinx slave SelectMap mode or through the JTAG cable. This utility was incorporated as previous heavy ion tests revealed functional interrupts that disabled the SelectMap port.

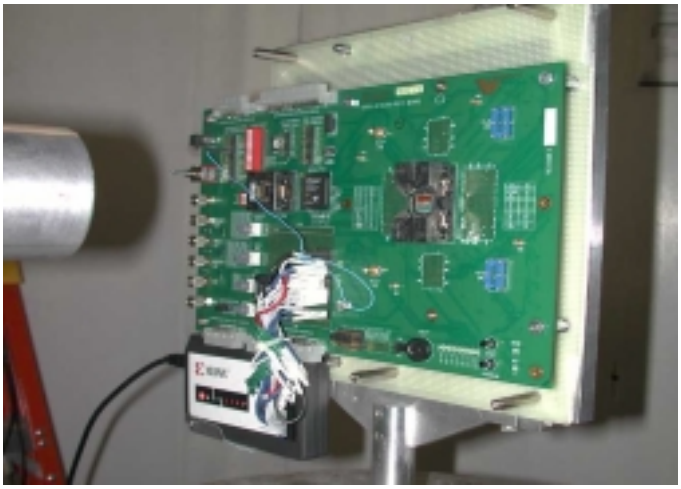

Fig. 3: *HW-AFXBG256-200* prototype board connected to the host PC and test software via Xilinx' MultiLinx cable in front of beam at Texas A&M.

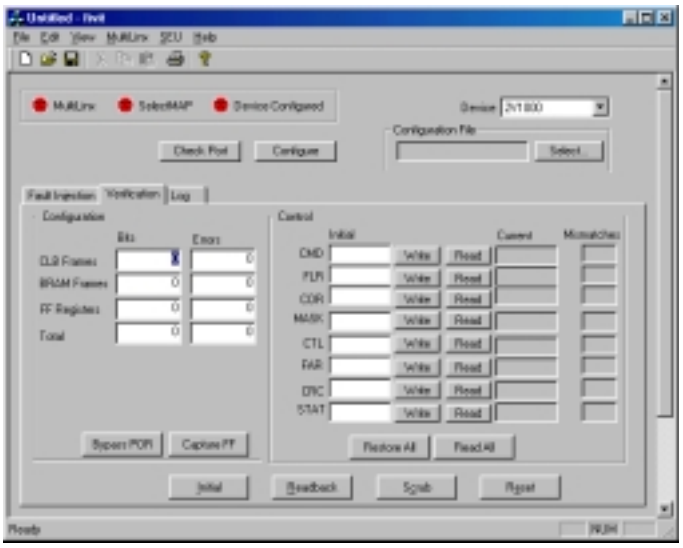

Figure 4: FIVIT (Fault Injection Verification Tool), a C++ based application used to check communication between the DUT and the software as well as determine the number of upsets in various memory cells and registers after each subsequent configuration and beam run.

III. TEST RESULTS

Each static test observed and counted upsets for one or more of the following elements: configuration memory, block SelectRam and user flip-flops and latches. In addition to upsets in these user elements, a number of single-event functional interrupts (SEFI) were noted. Heavy ions altering the logic states of the power-on-reset (POR) circuitry and SelectMap port were two of the more frequently occurring SEFIs, either disabling the communication between the FIVIT software or resetting the device. As more functionality was added to FIVIT with each successive test, greater visibility and control over the device was obtained and a few other types of SEFIs were discovered. More mention of this is made in sub-section "B. Static Configuration, block SelectRam & Flip-Flops Test."

A. Static Configuration Memory Test

The design implemented in the FPGA is a shift register design that automatically loads an alternating pattern until it is full. The capacity of the shift register used is (320x32) 9920 flip-flops. When verify is used in the 'IMPACT' program, the number of bit-flips in the configuration memory array is determined. The configuration memory cell SEU response is fitted to a physically based model presented by Larry Edmonds [3]. The equation used to fit the data is

$$\sigma = \sigma_{sat}\exp(-(L_{1/e}/LET)) \quad (1)$$

where σ_{sat} (a fitting parameter) is the saturation cross-section and $L_{1/e}$ (another fitting parameter) is the LET at which the cross section is 1/e times the saturation cross-section. To add a measure of conservatism, the fits (here and other test results to follow) have been adjusted upwards slightly to enclose as many data points as possible. Note that although both $L_{1/e}$ and σ_{sat} from this experiment are slightly lower than the results reported in the next section, the curves and data are reasonably consistent. The $L_{1/e}$ value for configuration memory cells was found to be approximately 5.5 MeVcm^2/mg with a saturation cross section of 4.25 E-8 cm^2/bit (Fig. 5). This $L_{1/e}$ value is slightly lower when compared to configuration memory bits at a later test. This is probably due to the lower range of LETs used to test the device as well as early test methods that had less visibility on the actual number of bits examined for upset.

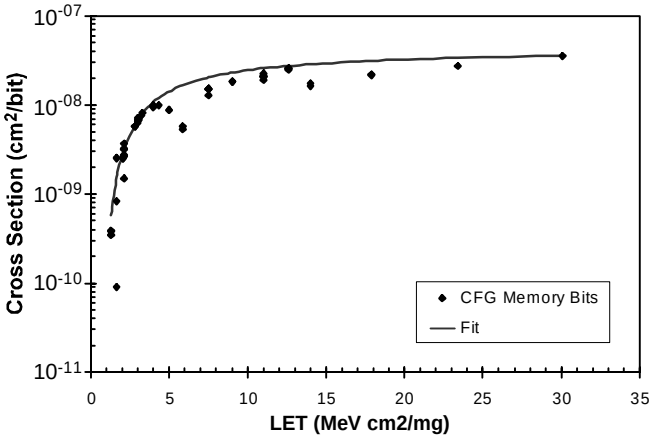

Figure 5: Cross-section vs. effective LET curve for configuration memory bits measured using the IMPACT program.

B. Static Configuration, Block SelectRam & Flip-Flop Test

In this test method, FIVIT is implemented for the first time; used for measuring errors in the configuration memory, block SelectRam cells and user flip-flops. SEFIs as a result of an ion hit to the POR and SelectMap circuitry were also identified through their failure signatures. As ions contact the device during the beam run, DUT current increased as errors were generated. A sudden high decrease of the DUT current to its starting value would indicate a POR. Meanwhile, meaningless data in all of the configuration registers was identified as a SelectMap error where communication had been lost and invalid data was being obtained. The use of FIVIT also granted the user two new abilities: to turn the POR bypass to either 'ON' or 'OFF', hence enabling or disabling the POR as well as setting the flip-flops to either '1s' or '0s'. Results indicate that when the POR bypass is turned 'ON', the likelihood of a POR error is 16% less than if it was turned off. In addition, ion strikes to the SelectMap also seem to lessen when POR bypass is turned 'ON', about 27%. A 7% disparity between flip-flops set to '0s' or '1s' also exist for POR and SelectMap and may not be statistically significant.

Most SEFIs seen for these tests were categorized as either POR or SelectMap errors. Adding an option of reading and writing to the configuration registers through either the MultiLinx or JTAG cable enabled and determined that 27% of the SelectMap errors were recoverable by first writing correct values into the CRC register through the JTAG cable. Some secondary SEFIs seen include ion strikes to cause a power down to the device or affecting configuration registers to be able to neither read or write, both occurrences which were infrequent and require further testing to obtain good cross sections. Other types of errors that occurred but do not lead to functional interrupts comprise of bit flips to configuration registers such as the frame length register (FLR), configuration option register (COR), and frame address reader (FAR). These errors were correctable and valid data is obtained from the readback. The cross section curves for the major upset modes are displayed in the following graphs (Fig. 6 – 10).

Data from two separate test trips utilizing the same test methodology were combined to produce the following test data with the exception of Fig. 8, which represents only the later test. Using the calculated (σ_{sat}) saturation cross- section and $L_{1/e}$ values, upsets rates were calculated for galactic cosmic rays in interplanetary space shielded by 100 mils of aluminum during the solar minimum time period. The rates were calculated using the RPP model to incorporate the response to ions impinging at all angles. An aspect ratio of 1/5 (for lateral dimension to collection depth) was used. Sensitivity analysis showed the result was changed only a little for other assumed aspect rations. Thus, "cosine law" response gives about the same rates. These upset rates are for heavy ions only and do not account for SEUs resulting from proton radiation. Upset rate values are shown on Table 1.

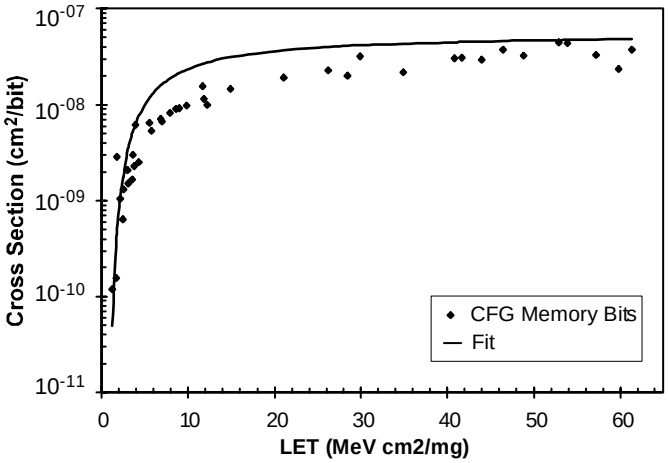

Figure 6: Cross-section vs. effective LET for configuration memory cells using new program, FIVIT. Saturation cross-section σ_{sat} is 5.5E-8 cm^2/bit and $L_{1/e}$ is 8.5 MeVcm^2/mg.

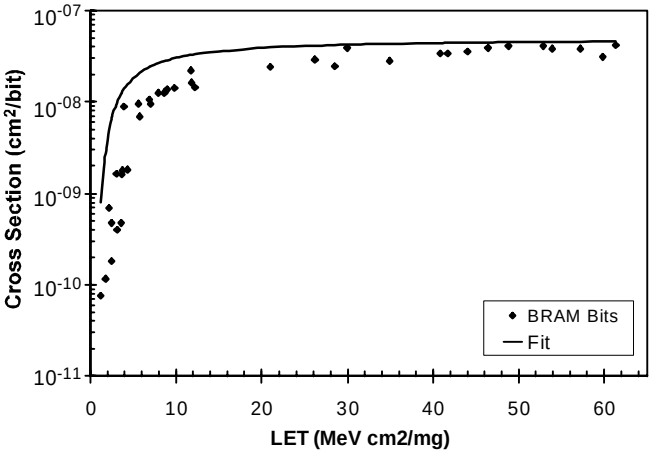

Figure 7: Cross-section vs. effective LET for block RAM memory cells. Saturation cross-section (σ_{sat}) is 5E-8 cm^2/bit and $L_{1/e}$ is 5 MeVcm^2/mg.

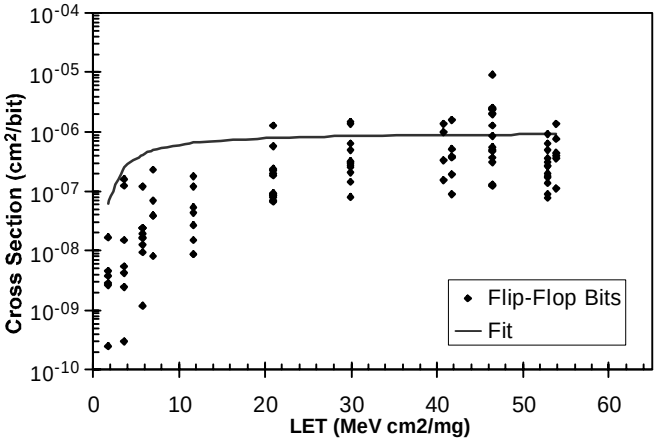

Figure 8: Cross section data points plotted as raw data. Varied scattering will be further investigated in next test.

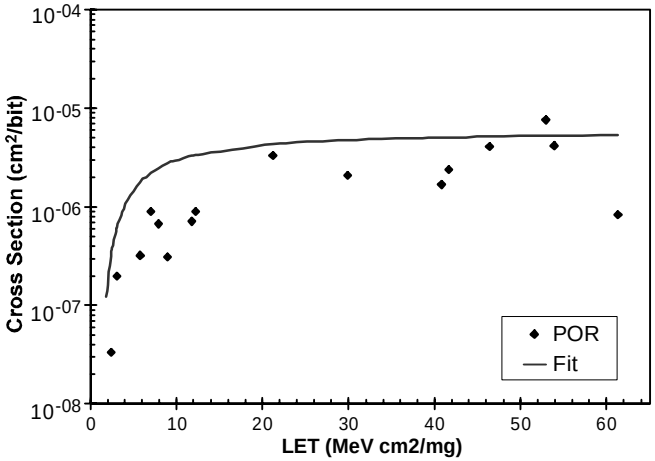

Figure 9: Cross-section vs. effective LET for POR SEFIs. Saturation cross-section σ_{sat} is 6E-6 cm^2/device and $L_{1/e}$ is 7 $MeVcm^2$/mg.

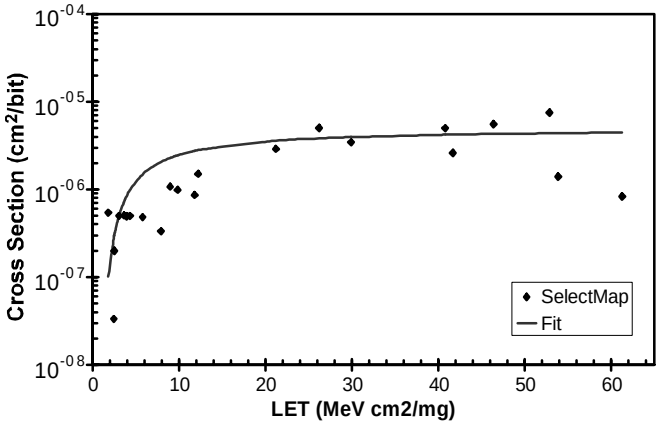

Figure 10: Cross-section vs. effective LET for SelectMap SEFIs. Saturation cross-section σ_{sat} is 5E-6 cm^2/device and $L_{1/e}$ is 7 $MeVcm^2$/mg.

Table 2. Virtex II Cross Section parameters and Upset Rates

	Configuration Memory		**Block SelectRam**		**Flip-Flops**		**POR SEFI**		**SelectMap SEFI**	
	$L_{1/e}$ ($MeVcm^2$/mg)	σ_{sat} (cm^2/bit)	$L_{1/e}$ ($MeVcm^2$/mg)	σ_{sat} (cm^2/bit)	$L_{1/e}$ ($MeVcm^2$/mg)	σ_{sat} (cm^2/device)	$L_{1/e}$ ($MeVcm^2$/mg)	σ_{sat} (cm^2/device)	$L_{1/e}$ ($MeVcm^2$/mg)	σ_{sat} (cm^2/device)
Test B	8.5	5.5E-8	5	5E-8	5	1E-6	7	6E-6	7	5E-6
Upset Rates*	4.4E-7/bit-day		1.1E-6/bit-day		2.1E-5/bit-day		7.0E-5/device-day		5.8E-5/device-day	

IV. Discussion

The test results of this radiation characterization for the *Virtex II* under static conditions demonstrate upset rates at 4.4E-7/bit-day for configuration memory cells and 1.1E-6/bit-day for block RAM cells. The data for flip-flop static SEU response is scattered and will require further testing and investigation in the next test. In addition, POR SEFIs are projected at 7.0E-5/device-day and 5.8E-5/device-day for Select Map related SEFIs. Saturation cross section and $L_{1/e}$ were 4.251E-8 cm^2/bit and 5.5 $MeVcm^2$/mg respectively for the first static upset test conducted with the IMPACT tool. These values were slightly lower than the values obtained from subsequent tests but nonetheless exhibit the same cross section trend. Some current increases were noted throughout these experiments but no latch-ups were observed.

Two major SEFIs have been established, the POR SEFI and the SelectMap SEFI, where the POR SEFI resets the FPGA, erasing all prior configuration bitstreams and the SelectMap SEFI, which requires a re-configuration of the DUT before communication is re-established again.

V. Conclusion

Further testing in the months ahead has been scheduled to study upsets during dynamic operations of this Virtex II device and the epitaxial version when it becomes available. Dynamic testing requires real-time configurations monitoring and, of necessity, will validate the monitoring technique, if successful. Additional error mitigation, including configuration scrubbing and triple-modular redundancy (TMR) of the target design, may be needed for critical space applications. We intend to test the efficacy of these in future dynamic test campaigns.

ACKNOWLEDGMENTS

The authors wish to thank Geoff Woodcock of UB Computer Service and Consulting for his development of the FIVIT program.

Special thanks are also given to Steve Guertin, Travis Minto, and Duc Nguyen for their technical support of this project.

REFERENCES

[1] C. Carmichael, "Proton Testing of SEU Mitigation Methods for the *Virtex* FPGA," *2001 MAPLD International Conference Proceedings*, vol. III, pp.23-25, September 2001.

[2] Xilinx, “Virtex II Platform Handbook,” © 2001. http://www.xilinx.com/products/virtex/handbook/index.htm

[3] L.D. Edmonds, “SEU Cross Sections Derived from a Diffusion Analysis,” IEEE Trans. Nucl. Sci., 43, 3207-3217, Dec. 1996.

[4] C. Carmichael, “Correcting Single-Event Upsets through Virtex Partial Reconfiguration,” Xilinx Application Note XAPP216, June 2000.